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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,692	12/04/2003	Jingkuang Chen	D/A1591D	8664

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EXAMINER	
SCHILLINGER, LAURA M	
ART UNIT	PAPER NUMBER
2813	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/727,692	CHEN ET AL.	
	Examiner	Art Unit	
	Laura M. Schillinger	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-13 and 17-24* is/are pending in the application.

4a) Of the above claim(s) *3 and 21-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1,4-13 and 17-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/31/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Newly submitted claims 23-24 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: Claims 23 pertains to a device including forming the heterogeneous devices on the same plane; Claim 24 pertains to a device including an SOI substrate wherein the heterogeneous devices are formed above the insulating layer. These claims constitute independent and distinct species from that of the originally elected claims which pertains to a device with wells formed in the silicon substrate

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 23-24 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Rejections - 35 USC § 112

Claims 13 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicant claim recites an "a plurality of homogeneous devices defined in the same substrate by an implantation" that include a CMOS and DMOS and goes on further to recite that a PD defined in the same substrate "by the same implantation". Upon review of Applicant's specification, it was found that over 6 ion implantations took place to form the

CMOS/DMOS/PD devices. The implantations used to in the specification which formed CMOS and DMOS regions on the substrate were not the same ion implantations used to define the PD. Rather the source/drain regions 148/158/146/156 of the CMOS/DMOS devices could be used to simultaneously form the PD. The Applicant's claim language requires that the CMOS/DMOS devices should be DEFINED by the same implantation as that which DEFINES the PD- which appears to contradict the Applicant's specification and therefore gives rise to new matter. Moreover, Applicant's language suggests a SINGLE implantation which is simultaneous- it is clear that for a photodiode to be defined at least an N and P implantation need to occur. This lack of clarity in the claim language gives rise to new matter. Claims 1,4-12, 17-20 depend from claim 13 and therefore are also rejected under 35 U.S.C. 112, first paragraph as failing to comply with the written description requirement.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 4-13 17-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakagawa et al ('065).

Nakagawa teaches the following claimed limitations:

1. (Previously Presented) The device of claim 13, further comprising: a high voltage well of a first circuit device defined in the substrate (305); and a first low voltage well of a second circuit device defined in the substrate (303) (Fig.28).

4. The device of claim 1, wherein the substrate comprises a layer of silicon (Col.8, lines: 50-60).

5. (Original) The device of claim 4, wherein the layer of silicon comprises p- type silicon (Col.8, lines: 50-60).

6. (Original) The device of claim 1, wherein the substrate comprises a silicon- on-insulator wafer comprising a single-crystal-silicon layer, a substrate and an insulator layer therebetween (Col.7, lines: 35-60).

7. (Original) The device of claim 6, wherein the single-crystal-silicon layer comprises p-type silicon (Col.8, lines: 50-60).

8. (Original) The device of claim 1, further comprising a second low voltage well of the second circuit device defined in the substrate (Fig.34 (305))

9. (Original) The device of claim 8, further comprising a field oxide layer over at least part of each of the high voltage well, the first low voltage well and the second low voltage well (Fig.34 (325)).

10. (Original) The device of claim 9, further comprising a polysilicon gate associated with each of the high voltage well, the first low voltage well and the second low voltage well (Fig.37D (351)).

11. (Original) The device of claim 10, further comprising:

a P-body defined in the high voltage well of the first circuit device (305);

an N+ source/drain defined in each of the P-body, the high voltage well and the first low voltage well of the second circuit device (307); and

a P+ source/drain in each of the P-body and the second low voltage well of the second circuit device (324) (Fig.34) and Col.15, lines: 50-65).

12. (Original) The device of claim 11, further comprising:

a passivation oxide layer over at least the field oxide layer and the polysilicon gates (Fig.37D (352);

a plurality of vias through the passivation oxide layer; and a plurality of contacts, each of the contacts extending through the vias and contacting at least one of the sources/drains (inherent-need contact holes to form source/drain contacts) (Co.15, lines: 50-65).

13. (Previously Presented) A heterogeneous device, comprising:

a substrate (Fig.13A (51));

a plurality of heterogeneous circuit devices defined in the same substrate the plurality of heterogeneous circuits comprises a CMOS and a DMOS (Fig.12D) and Col.8, lines: 30-40 and Col.15, lines: 60-65). (Fig.13A); and

a photodiode defined in the same substrate by the same implantation (Fig.13A (PD)- Col.8, lines: 50-68- teaching 1) that the chip 1 has one or more elements formed thereon in the same manner as in other embodiments (CMOS/DMOS) and teaches the doping formation of the PD).

17. (Original) The device of claim 13, wherein the substrate comprises a layer of silicon (Fig.13A (51)).

18. (Original) The device of claim 17, wherein the layer of silicon comprises p-type silicon (Fig.13A (51) and Col.8, lines: 50-60).

19. (Original) The device of claim 13, wherein the substrate comprises a silicon- on-insulator wafer comprising a single-crystal-silicon layer, a substrate and an insulator layer therebetween (Col.7 lines: 35-60).

20. (Original) The device of claim 19, wherein the single-crystal-silicon layer comprises p-type silicon (Col.8, lines: 50-60).

Response to Arguments

Applicant's arguments filed 12/7/06 have been fully considered but they are not persuasive. Applicant argues that the DMOS/CMOS and PD are taught in different embodiments and are not taught to be combined together on the same substrate- this is not persuasive since Nakagawa teaches on Col.8, lines: 50-65- that the chip has one or more elements formed thereon in the same manner as other embodiments- thus supporting the idea that the CMOS and DMOS taught in other embodiments may be combined to be formed on the same substrate. Moreover, Applicant argues that Nakagawa fails to teach the devices being all defined by the same implantation. As explained above in the Examiner's 112 rejection, this argument is not persuasive because Applicant's own specification fails to teach an implantation that defines all the devices at the same time- rather it teaches to form the source/drain regions along with the photodiode regions simultaneously. This is not in the Applicant's claim and it is not taught by Nakagawa but it is not claimed.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

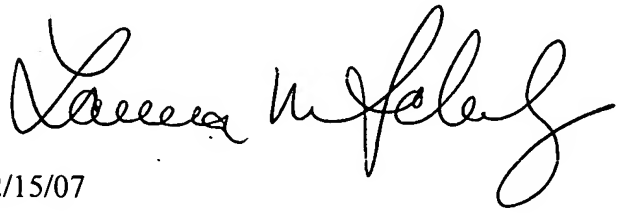
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laura M. Schillinger whose telephone number is (571) 272-1697. The examiner can normally be reached on M-T, R-F 7:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Laura M Schillinger
Primary Examiner
Art Unit 2813

02/15/07